Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **COLLECTOR Q1**
2. **COLLECTOR Q2**
3. **BASE Q2**
4. **EMITTER Q2**
5. **SUBSTRATE**
6. **BASE Q3**
7. **COLLECTOR Q3**
8. **EMITTER Q3**
9. **COLLECTOR Q4**
10. **BASE Q4**
11. **EMITTER Q4**
12. **EMITTER Q5**
13. **BASE Q5**
14. **COLLECTOR Q5**
15. **EMITTER Q1**
16. **BASE Q1**

**2 1 16 15 14**

**6 7 8 9 10**

**13**

**12**

**11**

**3**

**4**

**5**

**MASK**

**REF**

**5998A**

**NOTE: The substrate must be connected to a voltage which is more negative than any**

**collector voltage in order to maintain isolation between transistors and provide for**

**normal transistor action.**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: See note**

**Mask Ref: 5998A**

**APPROVED BY: DK DIE SIZE .050” X .050” DATE: 2/12/16**

**MFG: HARRIS/RCA THICKNESS .020” P/N: CA3083**

**DG 10.1.2**

#### Rev B, 7/19/02